## REMARKS/ARGUMENTS

Claims 1-36 are currently pending in this application.

***Allowable Subject Matter***

The Examiner is thanked for indicating that claims 2, 5, 7-9, 13, 16, 18-20, 27, 30 and 32-34 contain allowable subject matter if written in independent form.

***Claim Rejections - 35 USC §103***

Claims 23, 25, 26, 31, 35 and 36 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. patent No. 5,859,878 to Phillips et al. (hereinafter "Phillips"), in view of U.S. Patent No. 6,373,902 to Park et al. (hereinafter "Park").

The present invention is directed towards a serial bus processor coupled to memory-mapped registers of a programmable radio interface processor (RIP), configured to communicate between the digital section and the analog section of a wireless communications system. The serial bus processor receives data from a plurality of lookup tables which, in turn, are indexed by data received from the analog section. The serial bus processor then uses data values retrieved from the lookup tables to generate processed control data for controlling the digital module. The lookup tables are programmed with data to compensate for nonlinearities

which may be present in the analog section, but are not accounted for in the digital section.

Phillips discloses a digitally programmable transmit module in a radio device including an analog sub-module and digital processing sub-module. Phillips fails to disclose a plurality of lookup tables which are indexed by data received from the analog radio module, as is required by claim 23. Park discloses a device for linearizing a transmitter in a digital radio communication system. Park further discloses a plurality of lookup tables, which are indexed by data received from the analog radio module. However, Park's tables do not disclose an "indexing" scheme as is required in claim 23.

Instead, the lookup tables of the present invention provide for "controlling the nonlinearities in the analog section" due to a lack of accounting for these nonlinearities in the "digital section". This feature is distinguished from the look up tables of Park because it permits "coupling any of a plurality of analog sections to any of a plurality of digital sections, irrespective of the specific electronic characteristics of the analog section." (See Background of the present application).

Based on the arguments presented above, since the combination of Phillips and Park do not teach or suggest all of the elements of claim 23, the Applicants respectfully submit claim 23 is allowable over the cited prior art. Further, claims 25, 26, 31, 35 and 36 depend on claim 25, and the Applicants believe these claims

are allowable for the same reasons provided above. Accordingly, withdrawal of the 35 U.S.C. §103(a) rejection of claims 23, 25, 26, 31, 35 and 36 are respectfully requested.

Claims 1, 3, 4, 6, 10-12, 14, 15, 17, 21, 22, 24, 28, and 29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Phillips et al. and Park, and further in view of U.S. Patent 5,768,695 to Fischer et al. (hereinafter "Fischer").

Fischer discloses an apparatus for providing a flexible interface for creating the necessary control signaling of a radio transmitter. This disclosure includes a radio interface unit and a register set coupled to a state machine. However, the combination of Fischer, Phillips and Park does not teach or, suggest the use of memory-mapped registers. Further, the Examiner, citing U.S. Patent No. 5,933,158 to Santos (hereinafter "Santos"), has suggested that it would have been obvious to one of skill in the art to use "memory mapped" registers as they are the fastest registers. However, the Applicants respectfully submit that the advantage gained in speed is also not disclosed in Santos. In fact, a close reading of Santos shows that the speed Advantage is actually achieved by the processor memory accesses and not the system of memory-mapped registers. Accordingly, the Applicants respectfully submit that the Examiner has improperly inferred the relative speed of memory-mapped registers from Santos, and claims 1 and 12 are allowable over the cited prior art. (*See* Santos, "An advantage of storing information in the system memory-

mapped registers is that the processor accesses these memory mapped registers with memory accesses, its fastest mechanism for data retrieval.")

Claims 3, 4, 6, 10-11, 14, 15, 17, 21, 22, are dependent upon claims 1, and 12, which the Applicants believe is allowable over the cited prior art of record for the same reasons provided above. Claims 24, 28, and 29 depend on claim 23 which the Applicants believe is allowable for the same reasons provided above.

Based on the arguments presented above, withdrawal of the 35 U.S.C. §103(a) rejection of claims 1, 3, 4, 6, 10-12, 14, 15, 17, 21, 22, 24, 28, and 29 are respectfully requested.

***Conclusion***

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

In view of the foregoing amendment and remarks, Applicants respectfully submit that the present application, including claims 1-36, is in condition for allowance and a notice to that effect is respectfully requested.

Respectfully submitted,

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